

IN THE UNITED STATES PATENT OFFICE

Applicant: Robert O. Conn
Assignee: Xilinx, Inc.
Title: "Bond and Back Side Etchback Transistor
Fabrication Process"

Serial No.: Not Yet Known File Date: April 14, 2004
Examiner: Not Yet Known Art Unit: Not Yet Known

Divisional of
Serial No.: 10/407,746 File Date: April 4, 2003
Docket No.: X-1322-1-1D US

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PRIORITY INFORMATION DISCLOSURE STATEMENT

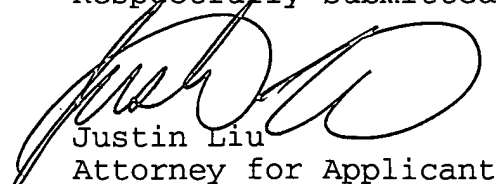
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the twelve (12) references listed in the attached Substitute for Form PTO-1449 (Information Disclosure Statement by Applicant).

All of these references were cited in prior related U.S. patent application Serial Number 10/407,746 filed April 4, 2003 to which this application claims priority. Copies of these references have not been supplied herein since they were previously submitted in the parent case.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully Submitted,


Justin Liu
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X-1322-1-1D US

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:** Assistant Commissioner for Patents, Washington, DC 20231.